Answers to Chapter 3 questions

Activity 3.1

Input values		Value	Value	Output	Value	Value	Output
A	B	$(a \cdot \overline{b})$	$(\overline{a} \cdot b)$	+	$(a + b)$	$\overline{(a \cdot b)}$	.
0	0	0	0	0	0	1	0
0	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	0	1	0	0

Both truth tables have the same output (columns 5 and 8). Hence both expressions are the same.

Activity 3.2

a

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

b

Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	0

c

Inputs			Output
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

d

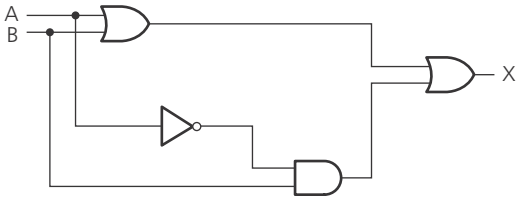
Inputs			Output
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

e

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

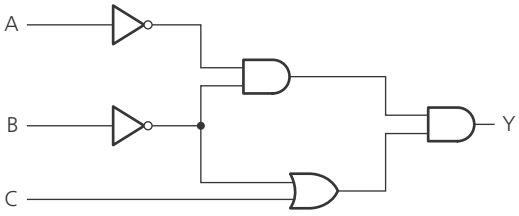
Activity 3.3

a X = 1 if (A = 1 OR B = 1) OR (A = 0 AND B = 1)



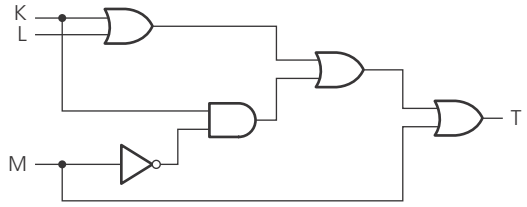
Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

b Y = 1 if (A = 0 AND B = 0) AND (B = 0 OR C = 1)



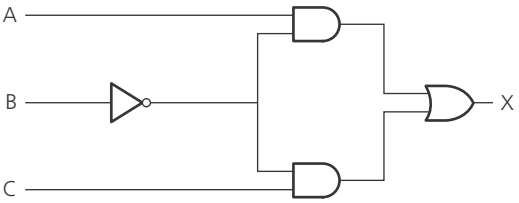
Inputs			Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

c T = 1 if (K = 1 OR L = 1) OR (K = 1 AND M = NOT 1) OR (M = 1)



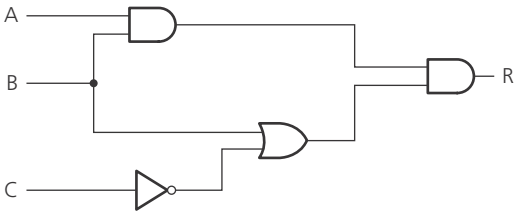
Inputs			Output
K	L	M	T
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

d $x = (a \cdot \overline{b}) + (\overline{b} \cdot c)$



Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

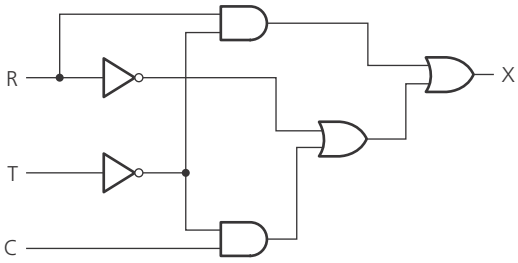
e R = 1 if (A = 1 AND B = 1) AND (B = 1 OR C = NOT 1)



Inputs			Output
A	B	C	R
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

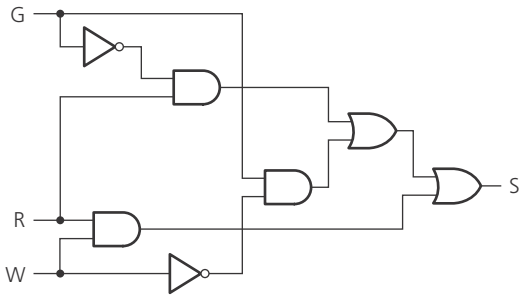
Activity 3.4

a X = 1 if (R = NOT 1) OR (C = 1 AND T = NOT 1) OR (R = 1 AND T = NOT 1)



Inputs			Output
R	T	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

b S = 1 if (G = 1 AND W = NOT 1) OR (G = NOT 1 AND R = 1) OR (W = 1 AND R = 1)



Inputs			Output
G	R	W	S
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Activity 3.5

First logic circuit:

Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

which confirms this as an AND gate.
Second logic circuit:

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

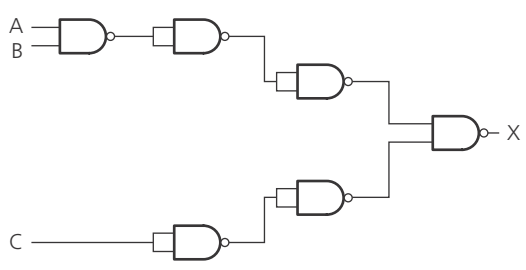
which confirms this as an OR gate.
Third logic circuit:

Input	Output
A	X
0	1
1	0

which confirms this as a NOT gate.

Activity 3.6

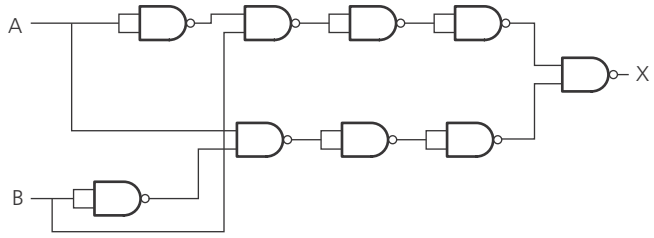
a



Inputs			Output from original circuit	Output from NAND gate only circuit
A	B	C		
0	0	0	1	1
0	0	1	0	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	1	1

which confirms that the two logic circuits have the same function.

b NAND-gate only circuit:



c This gives the following truth table:

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

which confirms that the logic circuit represents the XOR gate.

Activity 3.7

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

which is the truth table for the NOR gate.

Activity 3.8

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

which is the truth table for the NOR gate.

Activity 3.9

Inputs			Output
P	Q	R	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

which indicates that the logic circuit could be replaced by Input R only.